

SPICE Device Model Si4431CDY

Vishay Siliconix

P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

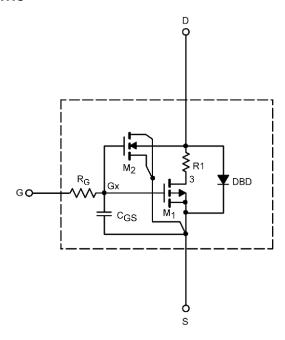
- · Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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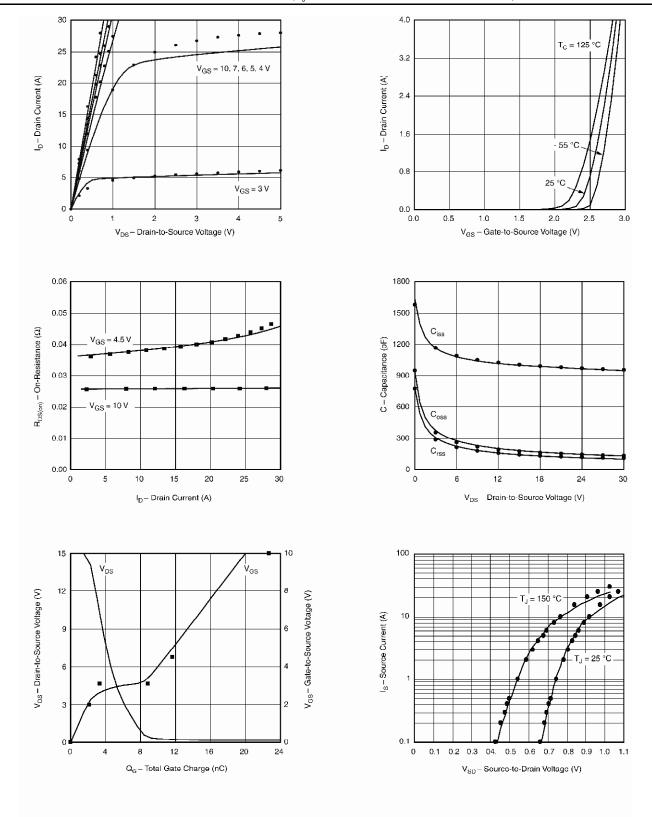
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	-				
Gate Threshold Voltage	$V_{_{\mathrm{GS(th)}}}$	$V_{_{DS}} = V_{_{GS}}, I_{_{D}} = -250 \ \mu A$	1.8		٧
Drain-Source On-State Resistance ^a	_	$V_{GS} = -10 \text{ V}, I_{D} = -7 \text{ A}$	0.026	0.026	Ω
	r _{DS(on)}	$V_{gs} = -4.5 \text{ V}, I_{D} = -5.6 \text{ A}$	0.037	0.037	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -7 \text{ A}$	10	18	S
Diode Forward Voltage	V _{SD}	I _s = -5.6 A	-0.81	-0.71	V
Dynamic⁵					
Input Capacitance	C _{iss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	1000	1006	pF
Output Capacitance	C _{oss}		183	180	
Reverse Transfer Capacitance	C _{rss}		144	145	
Total Gate Charge	Q_{g}	$V_{_{DS}} = -15 \text{ V}, \ V_{_{GS}} = -10 \text{ V}, \ I_{_{D}} = -7 \text{ A}$	20	25	nC
		$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -7 \text{ A}$	11	13	
Gate-Source Charge	Q_{gs}		3.5	3.5	
Gate-Drain Charge	Q_{gd}		5.5	5.5	

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA (T_=25°C UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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